

Figure 1 (Prior Art)

FIG. 2 is a block diagram of a network architecture showing a central adjunct processor connected to two switching fabrics, which in turn connect to various client devices and storage arrays.

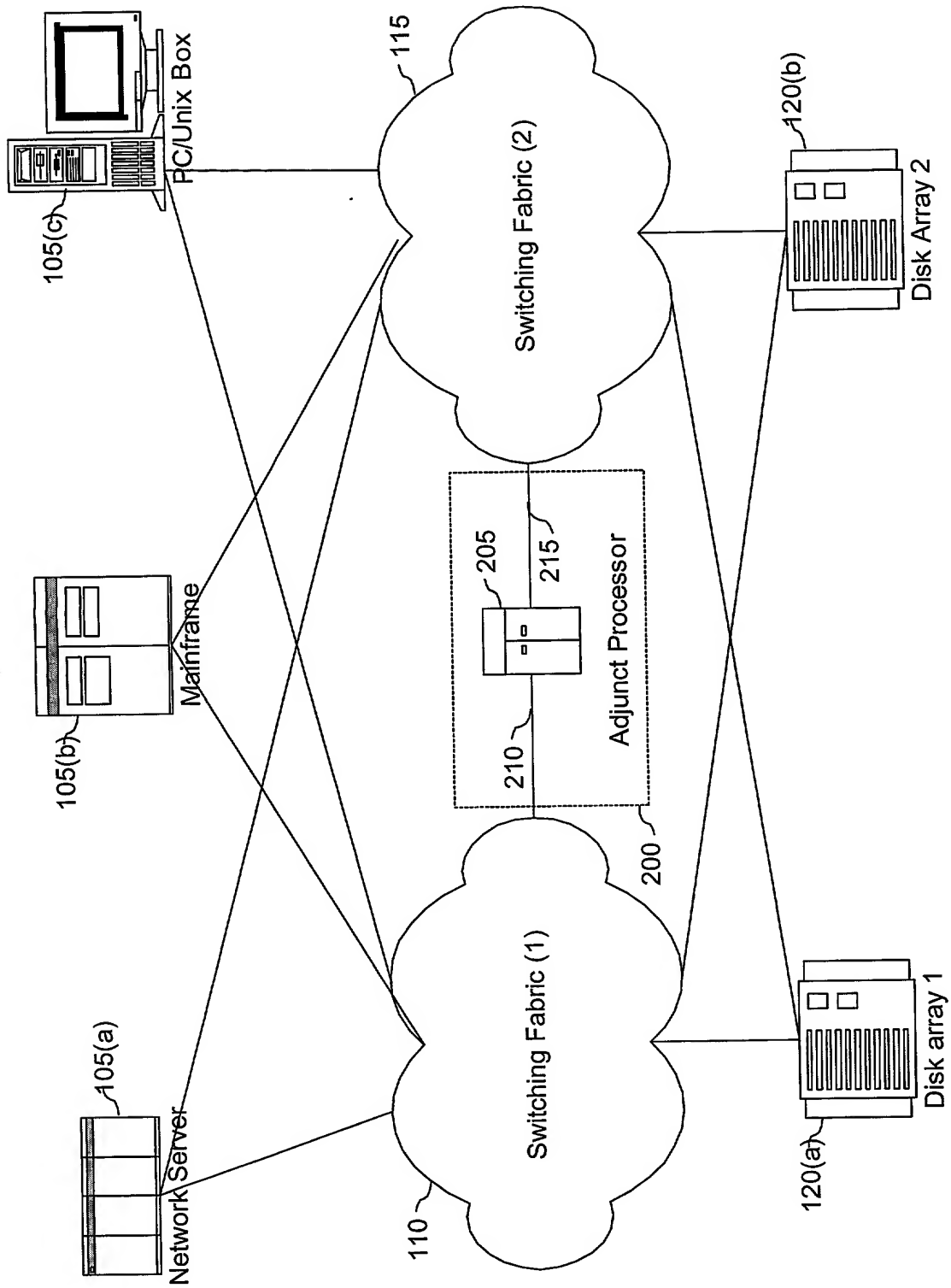


Figure 2

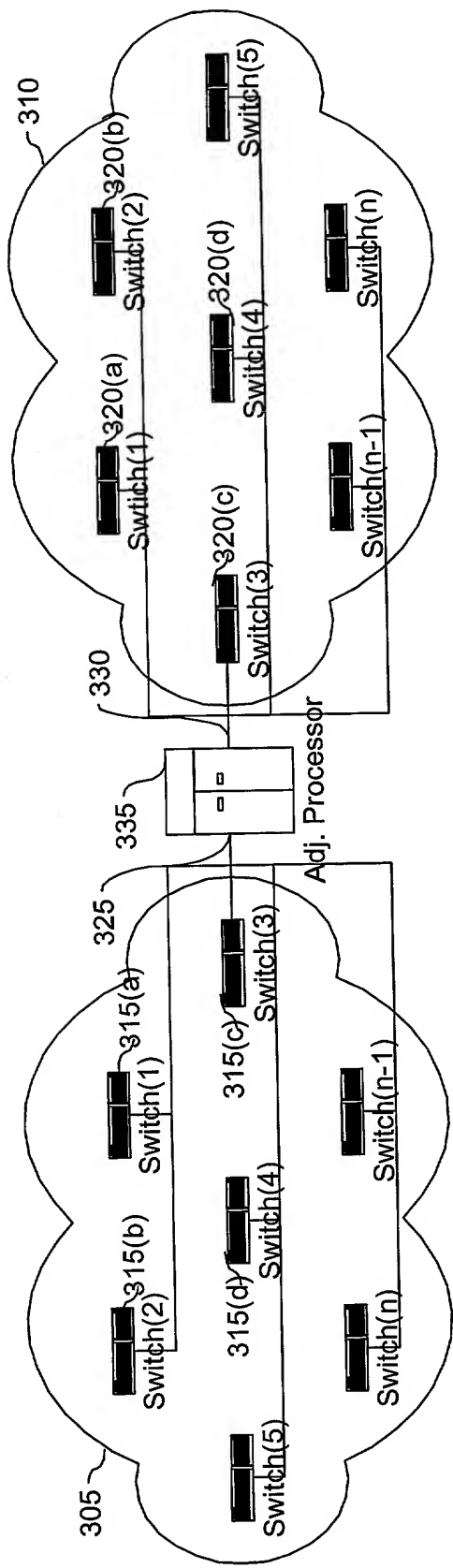


Figure 3A

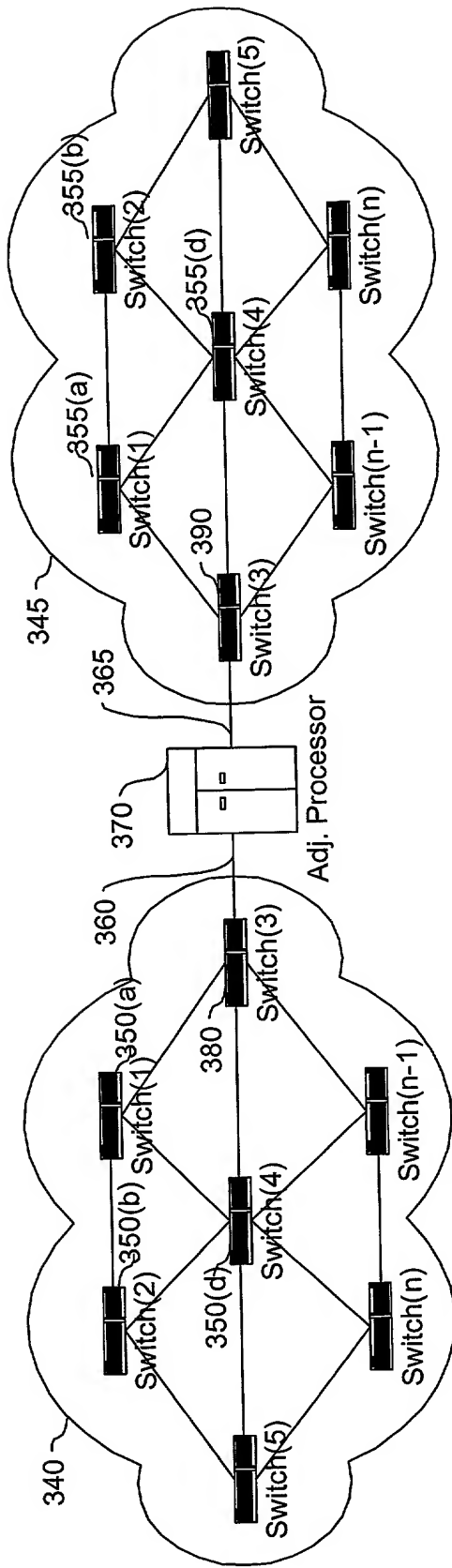


Figure 3B

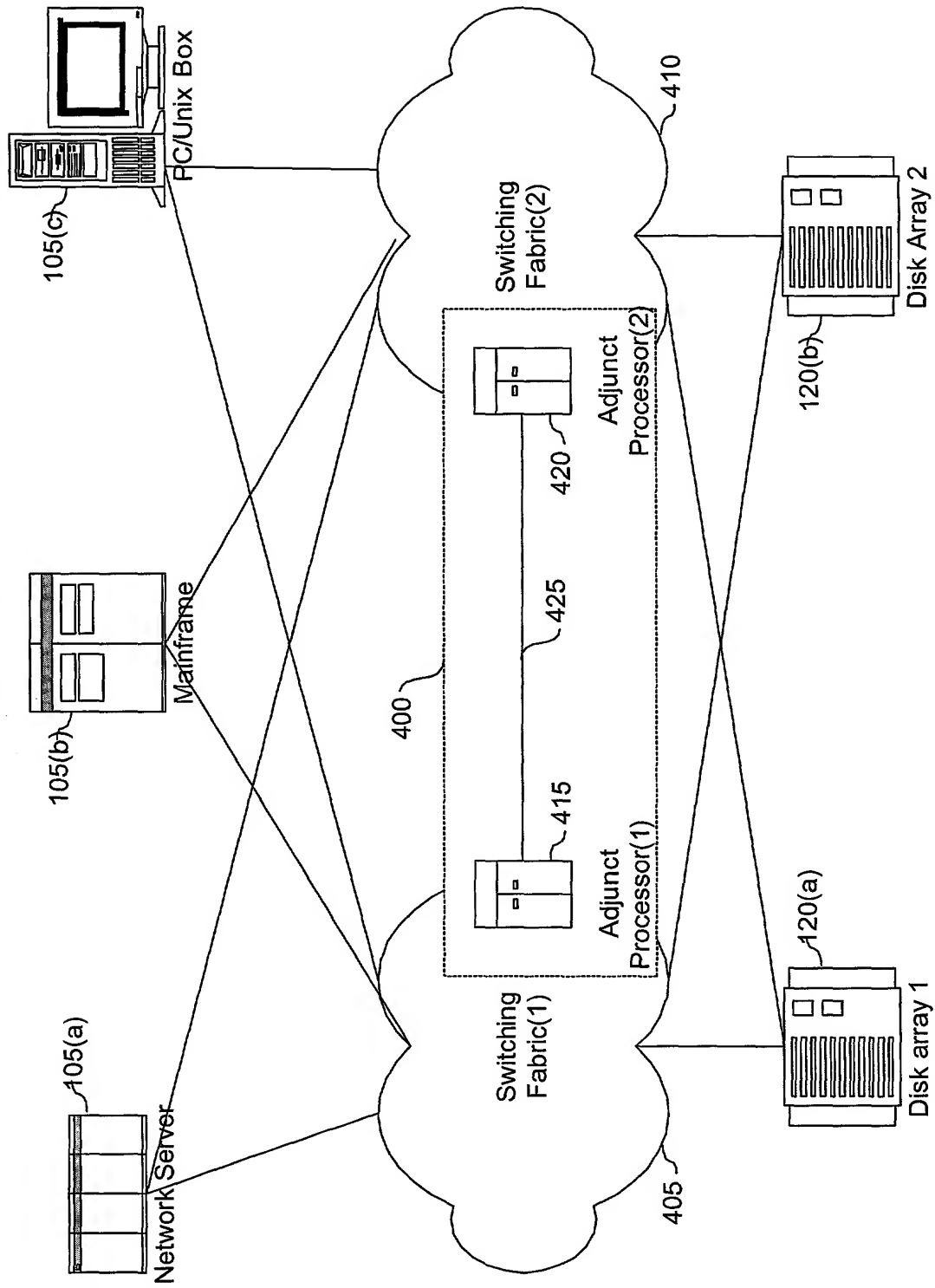


Figure 4

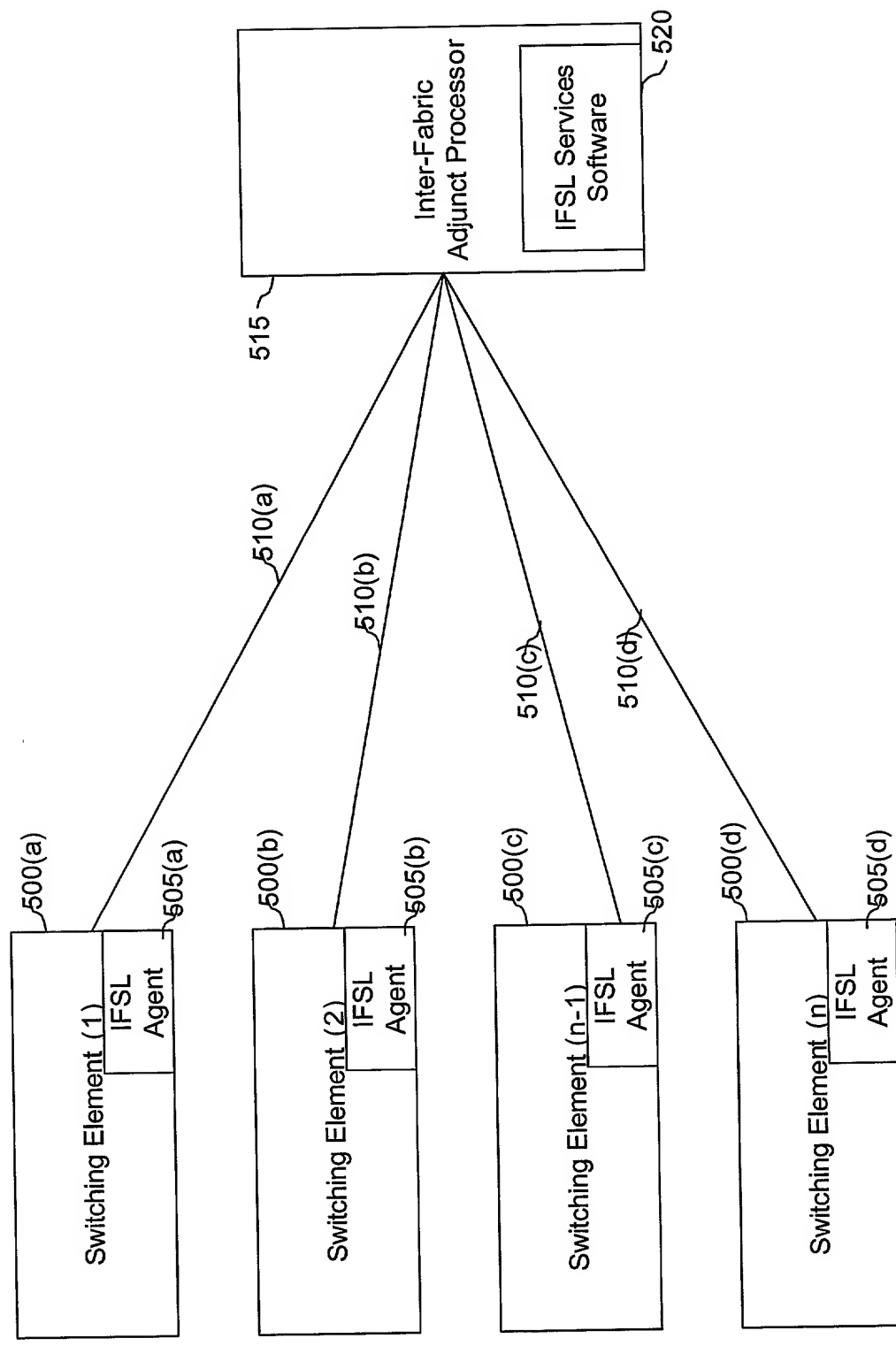


Figure 5

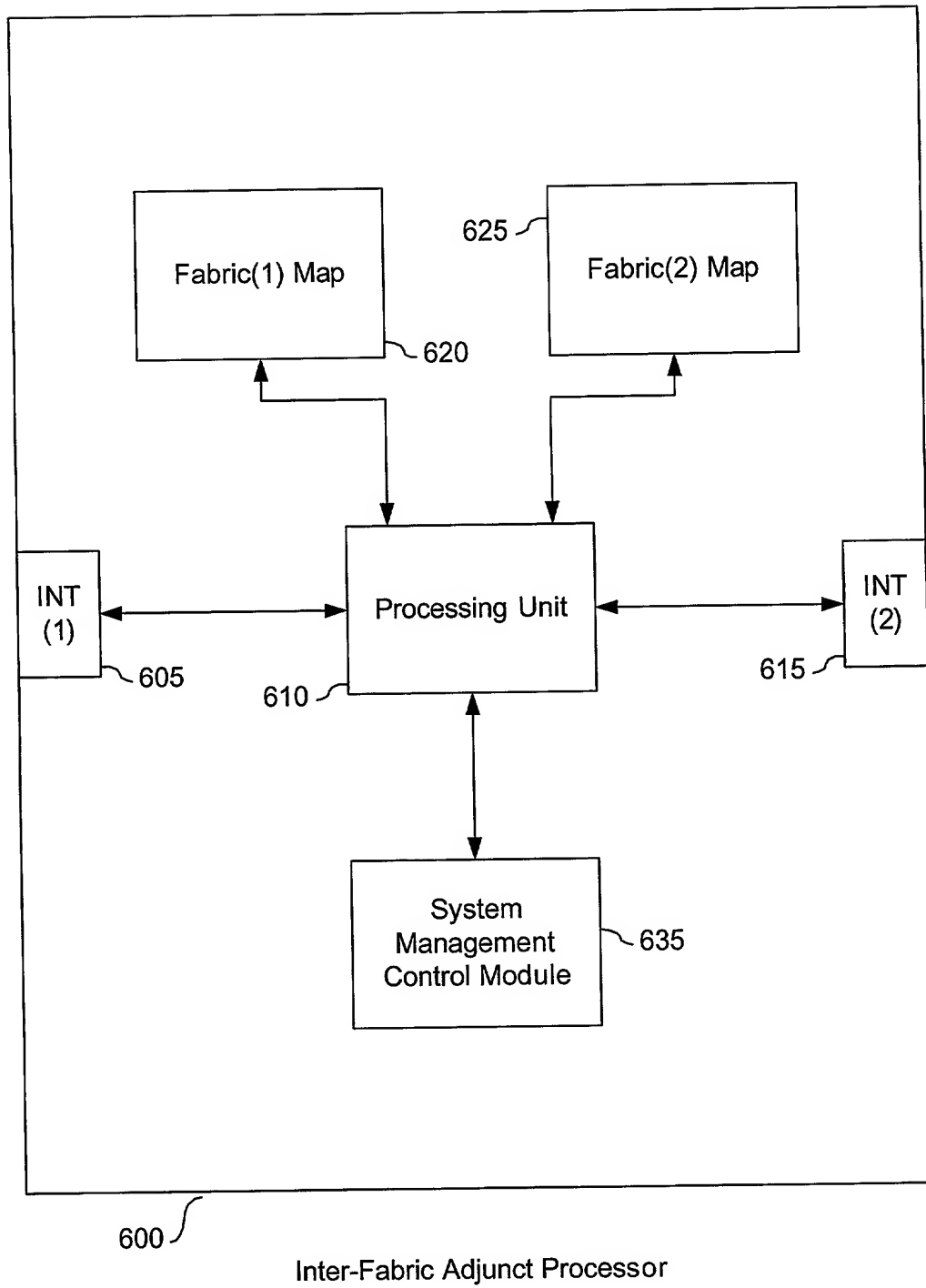


Figure 6

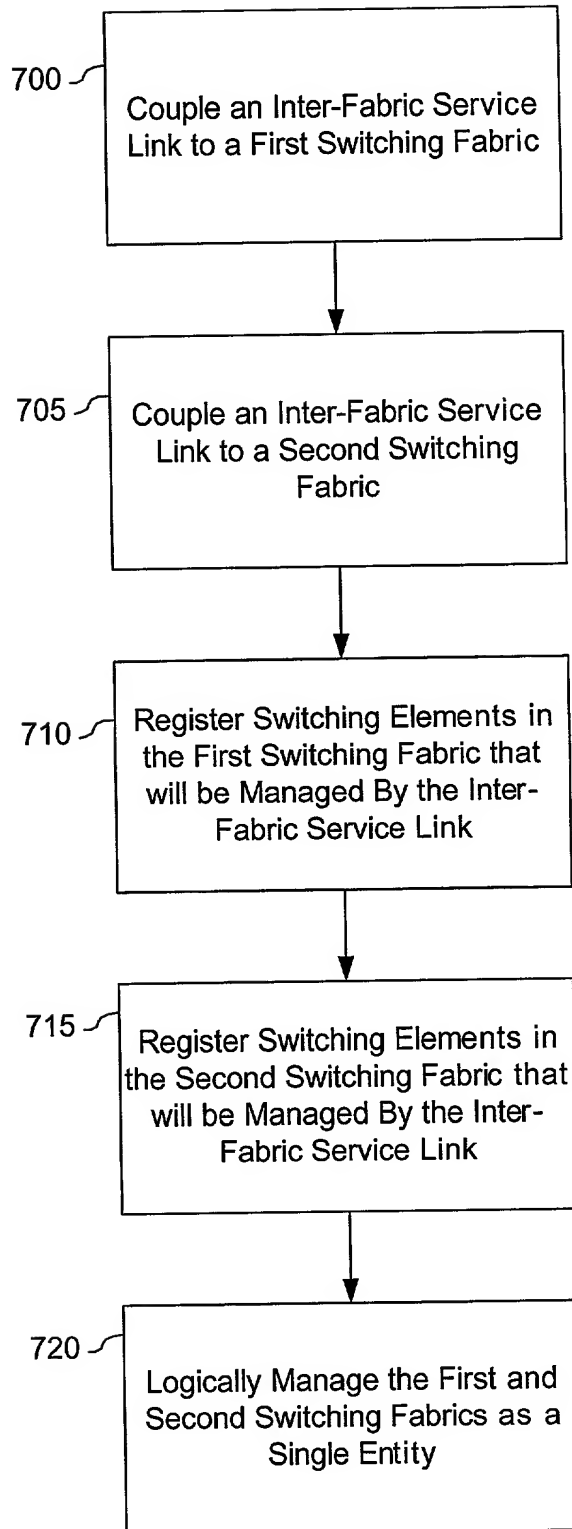


Figure 7

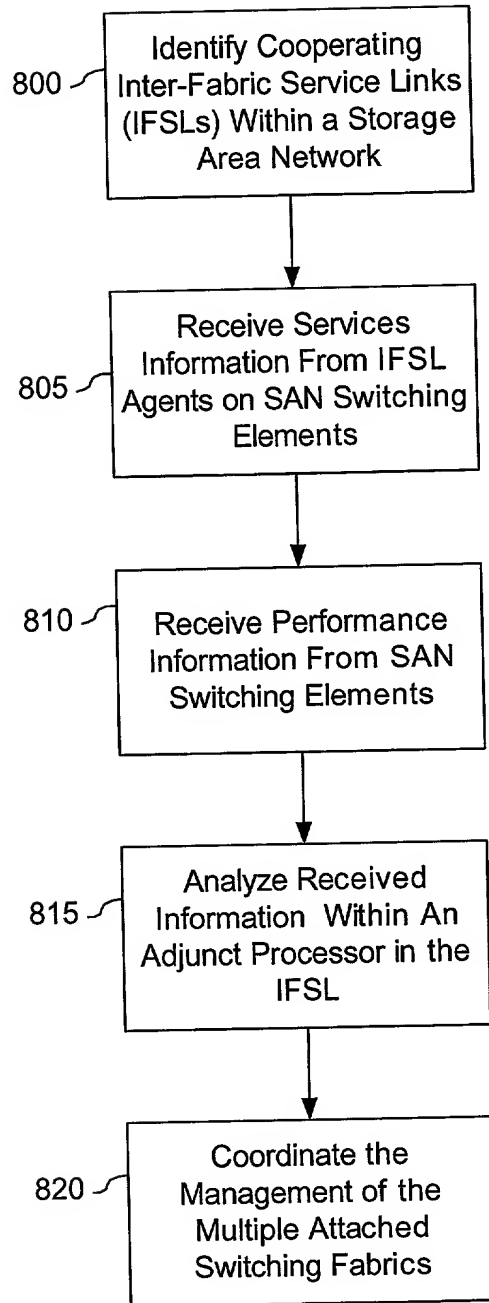


Figure 8



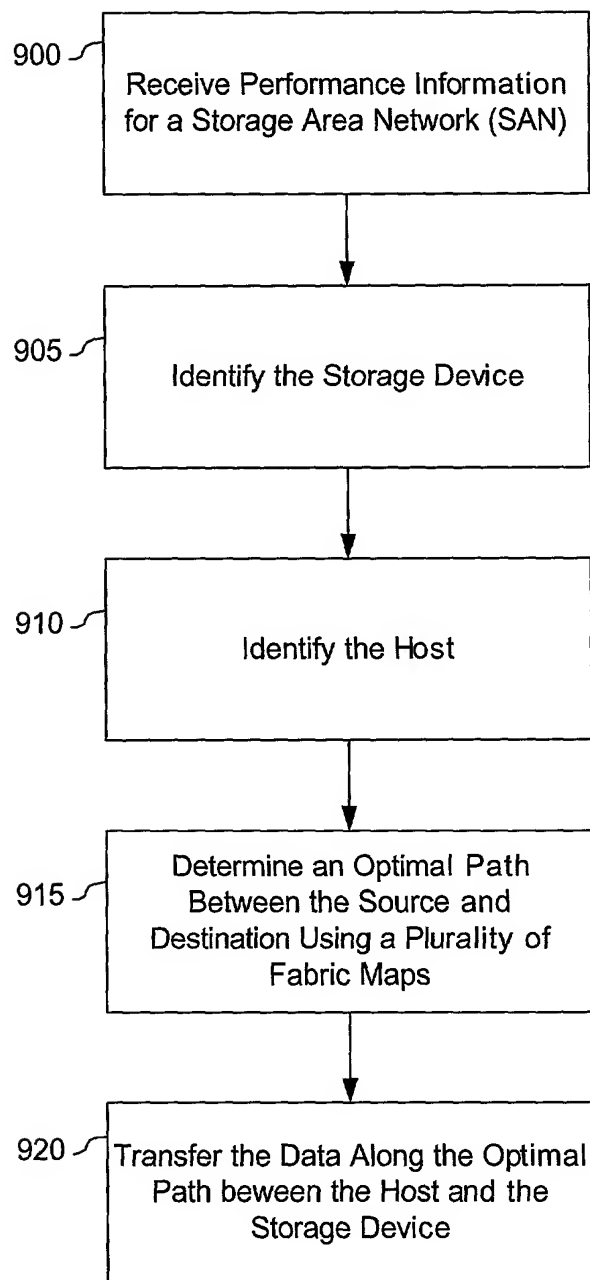


Figure 9